"KIOS" RESEARCH CENTER FOR INTELLIGENT SYSTEMS AND NETWORKS
SCHOOL OF ENGINEERING – UNIVERSITY OF CYPRUS

RESEARCH POSITION

The *Electronic Design, Test, and Reliability Laboratory* at the Electrical and Computer Engineering Department of the University of Cyprus announces a research position opening for a Research Assistant / PhD Candidate / Post-doctoral Researcher.

The *Electronic Design, Test and Reliability Laboratory* is part of the newly established "KIOS" Research Center for Intelligent Systems and Networks at the University of Cyprus (http://www.kios.org.cy). It conducts research in the areas of computer aided design, testing and reliability of modern VLSI circuits and systems. Research focuses on state-of-the-art CAD algorithms for automatic testing, diagnosis, and verification, applicable to large-scale VLSI circuits as well as reusable embedded cores integrated into whole chip-level architectures such as SoCs, NoCs, and large-scale on-chip multiprocessors. The Laboratory also has a strong interest in fault tolerance and reliability, especially for embedded systems and next-generation VLSI systems such as large-scale multicore chips. These activities are performed in close cooperation with the teams of the KIOS Research Center for Intelligent Systems and Networks, as well as numerous international research partners from academia and industry. The laboratory is extensively equipped, including high-end servers/workstations and state-of the-art CAD tools (Synopsys, Cadence, and Mentor Graphic) for development and simulation purposes, as well as several FPGA-based prototyping systems and high-end logic analyzers.

The hired researcher is expected to contribute, primarily, in the R&D activities of a newly funded project by the Cyprus Research Promotion foundation. The project investigates the design of reliable next-generation (hundreds to thousands of cores) manycore chips. In particular, it will investigate a resilient system architecture and operation, where both *design correctness* (HW verification) and *fabrication correctness* (manufacturing test) are performed *dynamically*, during the life-time of the chip, to enable the system to constantly detect errors, isolate and confine them, or tolerate them, thus, allowing it to adapt. Another important innovation of the proposed project is the investigation of *intelligent collaboration* between the system components to provide necessary feedback to the system and allow it to learn and adapt. The proposed system and methodologies will be evaluated using a simulation framework to be specifically developed for this purpose, as well as a prototype built using FPGA-based boards.

Prospective applicants must fulfill the following:

- Holder of a Bachelor's degree (B.Sc.) or a postgraduate degree (M.Sc or Ph.D.) in Computer Engineering or Electrical Engineering or Computer Science or a related discipline from an accredited institution.
- Sound knowledge in C/C++ software tool development. Skills in the areas of digital systems reliability, VLSI test and verification, computer architecture, electronic design automation, HW architecture simulation, and hardware description languages / SystemC will be considered especially beneficial.
- Excellent communication skills, must be able to collaborate effectively with various partners and be a team player.
- Good proficiency in oral and written English.

Our team-oriented working style and a cooperative leadership concept will give you the necessary freedom for your scientific research with a high degree of motivation, personal responsibility and creativity.

This position is on a contract basis, up to three years, which is renewable. Expected starting time is March 1st, 2009, or as soon as possible thereafter. Monthly salary depends on the candidate's qualifications and prior experience.

For more information, please contact:

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